

**Reducing the Cost & Complexity of Co-Packaged Optics**: Large-scale data transfers are becoming a critical bottleneck in modern high-performance computing (HPC) and data center architectures. While total throughput of the electrical interconnects has increased in recent years, to further increase it – while also addressing bandwidth density/energy efficiency challenges – co-packaged optics leveraging silicon photonics (SiPh) has emerged as a promising solution. In a typical co-packaged optics system, optical-electrical chiplets integrate the CMOS chip and SiPh photonic integrated circuit, while external laser sources supply the necessary light for signal transmission through a fiber connector attached to the chiplets. The current standard approach relies on polarization maintaining fiber (PMF) arrays between the external laser sources and the chiplets to ensure stable polarization states, required for optimal performance of the SiPh-based photonic devices. But while PMFs provide robust polarization control, they introduce significant drawbacks including high-precision alignment requirements, increased manufacturing complexity, and substantial packaging costs. At ECTC, NVIDIA researchers will describe an alternative approach that replaces PMFs with single-mode fibers (SMFs) to reduce cost and complexity without compromising system performance. They will present experimental results from a test chip demonstrating the viability of this solution, including a detailed cost-performance analysis comparing PMF- and SMF-based architectures.

* **The image above** is a schematic showing the optical path from the laser diode (LD) in an external laser source (ELS) module to the input of the co-packaged optics system (CPO).

**(Paper 2.6, “*All-SMF Arrays for Co-Packaged Optics: Optimizing Cost, Complexity and Performance,”* N. Mehta et al, NVIDIA)**